FIG.9

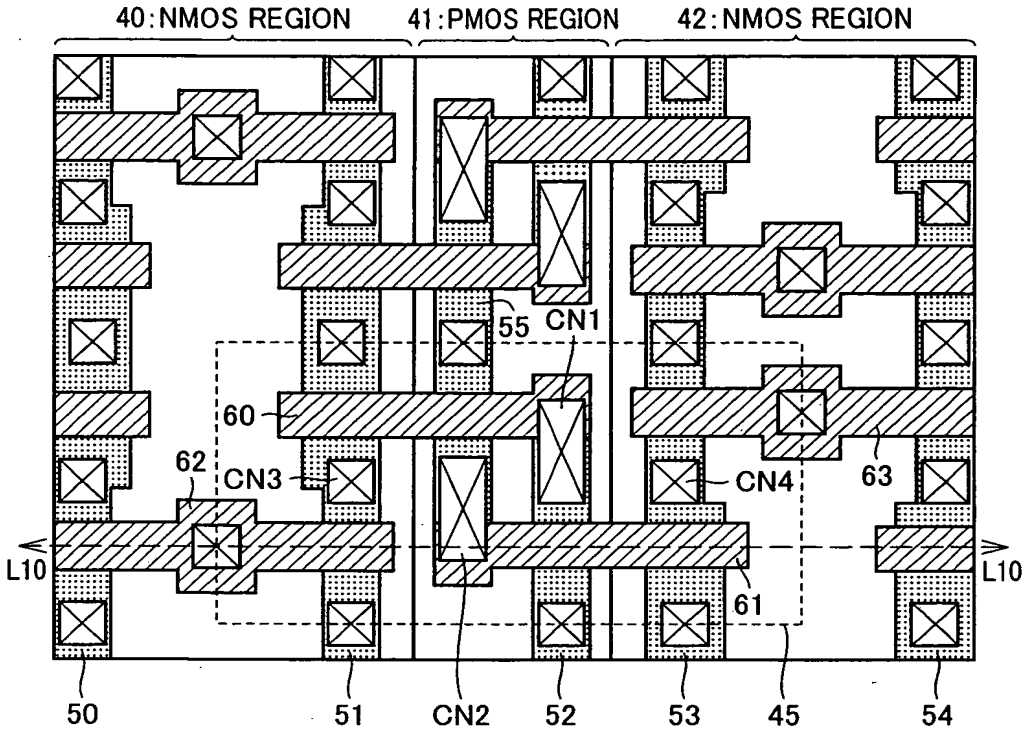

40:NMOS REGION
41:PMOS REGION
42:NMOS REGION
55
CN1
60
62
CN3
CN4
63
L10
L10
61
50
51
CN2
52
53
45
54

FIG.10

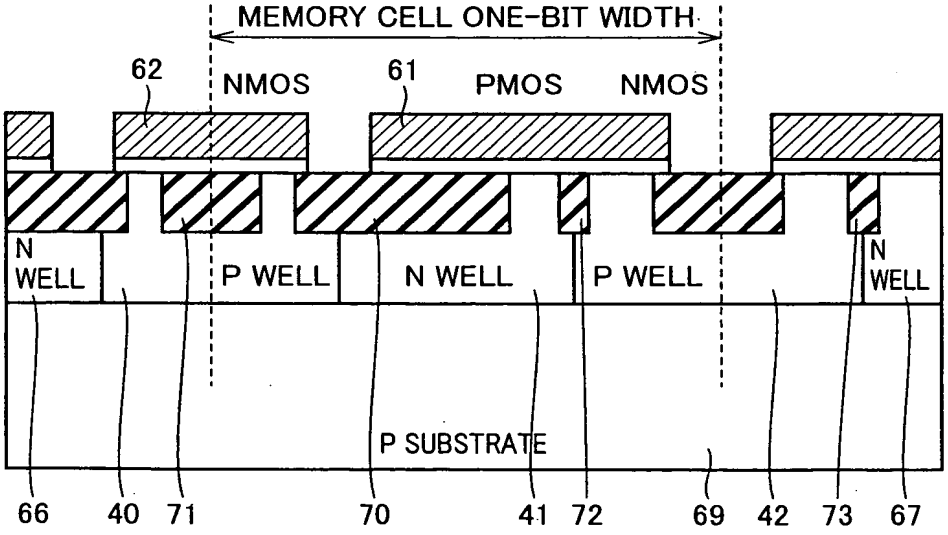

MEMORY CELL ONE-BIT WIDTH
62
NMOS
61
PMOS
NMOS
N WELL
P WELL
N WELL
P WELL
N WELL
P SUBSTRATE
66
40
71
70
41
72
69
42
73
67

FIG.13

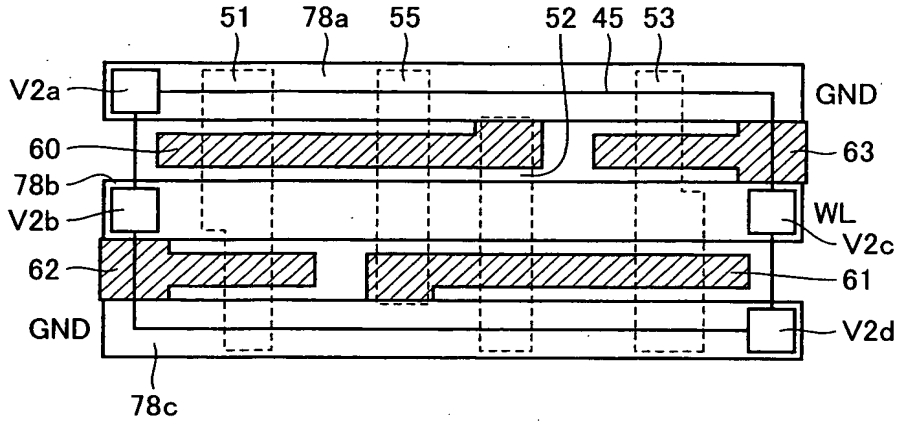
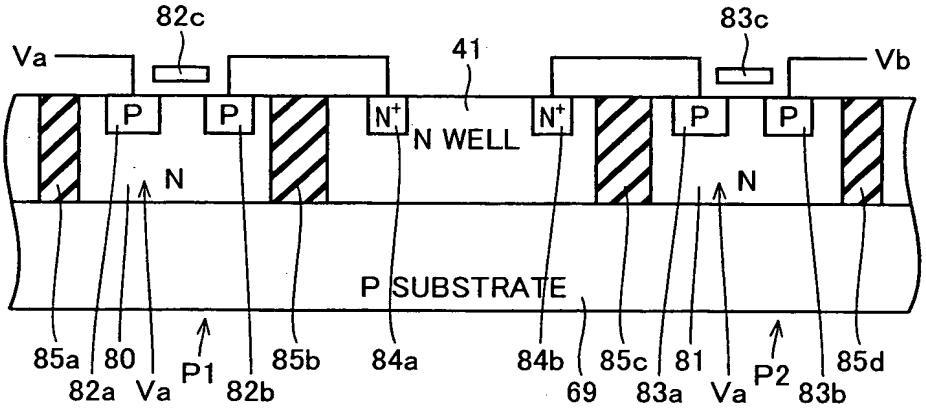

51
78a
55
52
45
53
V2a
GND
60
63
78b
V2b
WL
V2c
62
61
GND
V2d
78c

FIG.14


82c
83c
Va
41
Vb
P
P
N+
N WELL
N+
P
P
N
N
P SUBSTRATE
85a
80
P1
85b
84a
84b
85c
81
P2
85d
82a
Va
82b
69
83a
Va
83b